

**FIG. 2**

**FIG. 3A**

FIG. 3A is a cross-sectional view of a semiconductor device. The device includes a substrate 212 with a base layer 211. A gate stack 206 is formed on the substrate, comprising a gate electrode 207 and a gate insulating layer 208. A source/drain region 209 is located on the left, and a channel region 205 is on the right. A thin layer 203 is deposited over the gate stack. A layer 204 is formed on top of 203, with two small openings 210. A layer 202-1 is formed on the left, and a layer 202-2 is formed on the right. A layer 201-1 is formed on top of 202-1, and a layer 201-2 is formed on top of 202-2. A layer 300 is formed on top of 201-1 and 201-2. A layer 201 is formed on top of 201-1 and 201-2.